

JIS College of Engineering

PG-Curriculum & Syllabus of Electronics and Communication Engineering (VLSI & Embedded Systems) [MTech ECE (VLSI & ES)] 2026 Regulation

CURRICULUM 2026 Regulation

SEMESTER I

Sl. No.	Core/ Elective	Code	Subject	Contact Hours/ Week				
				L	T	P	Total	Credit points
1	Core 1	MEC101	CMOS Analog IC Design	3	0	0	3	3
2	Core 2	MEC102	Advanced Digital System Design	3	0	0	3	3
3	PE1	MEC103	A) Semiconductor Devices B) VLSI Process Technology C) Computer-Aided Design of Digital System	3	0	0	3	3
4	PE2	MEC104	A) MEMS and Microsystems B) Software for Embedded Systems C) Distributed Embedded Computing	3	0	0	3	3
5	MLC	MLC101	Research Methodology and IPR	2	0	0	2	2
	PRACTICAL							
6	Lab 1	MEC191	FPGA System Design Laboratory	0	0	3	3	2
7	Lab 2	MEC192	Analog and Digital CMOS VLSI Design Laboratory ,	0	0	3	3	2
	SESSIONAL							
8	Audit	MC101	A) Stress Management by Yoga B) Pedagogy Studies C) Constitution of India D) Personality Development through Enlightenment skills	2	0	0	2	0
				Total			22	18

** MLC – Mandatory Learning Course*

SEMESTER II

Sl. No.	Core/ Elective	Code	Subject	Contact Hours/ Week				
				L	T	P	Total	Credit points
1	Core 3	MEC201	SoC Design for Embedded Systems	3	0	0	3	3
2	Core 4	MEC202	VLSI Signal Processing	3	0	0	3	3
3	PE3	MEC203	A) VLSI Testing and Verification B) Low Power VLSI Design C) Digital System Design & FPGAs	3	0	0	3	3
4	PE4	MEC204	A) Advanced Embedded Systems B) Introduction to Embedded Controllers C) Embedded Programming	3	0	0	3	3
5	Minor Project	MEC281	Mini Project with Seminar	0	0	4	4	2
	PRACTICAL							
6	Lab 3	MEC291	Advanced Embedded Systems Lab	0	0	3	3	2
7	Lab 4	MEC292	VLSI Signal Processing Lab	0	0	3	3	2
	SESSIONAL							
8	Audit	MC201	A) English for Research Paper Writing B) Disaster Management C) Sanskrit for Technical Knowledge	2	0	0	2	0
				Total			24	18

SEMESTER III

Sl. No.	Core/ Elective	Code	Subject	Contact Hours/ Week				
				L	T	P	Total	Credit points
1	PE5	MEC301	PROGRAM SPECIFIC ELECTIVE-V: ASIC Design (Credit can be earned from the Swayam/NPTEL course as mapped by BOS)	3	0	0	3	3
2	OE	MEC302	A) Business Intelligence & Analytics (Swayam/NPTEL) B) Industrial Safety Engineering (Swayam/NPTEL)	3	0	0	3	3
3	Major Project	MEC381	DISSERTATION/RESEARCH PROJECT/INTERNSHIP (PART-1)	0	0	28	28	14
				Total			34	20

SEMESTER IV

Sl. No.	Core/ Elective	Code	Subject	Contact Hours/Week				
				L	T	P	Total	Credit points
	SESSIONAL							
1	Major Project	MEC481	DISSERTATION/RESEARCH PROJECT/INTERNSHIP (COMPLETION- PART- II)	0	0	40	40	20
				Total			40	20

Total Credit = 76 (18+18+20+20)

SEMESTER I

Paper Name: CMOS ANALOG IC DESIGN
Paper Code: MEC101
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

1. The course will discuss the equivalent circuits and models of MOS circuits.
2. To analyze bias circuits using CMOS current mirrors.
3. To design and analyze the frequency response of multistage differential amplifiers.
4. To discuss the stability and frequency compensation of feedback amplifiers.

MODULE I SINGLE STAGE AMPLIFIERS 6L

Review of MOS physics and equivalent circuits and models. Large and Small signal analysis CS, CG and source follower, miller effect, frequency response of CS, CG and source follower.

MODULE II CURRENT MIRRORS 6L

Current Sources, Basic Current Mirrors, Cascode stages for Current mirrors , Wilson Current Mirror, Large and small signal analysis of current mirrors.

MODULE III MULTISTAGE DIFFERENTIAL AMPLIFIERS 10L

Differential amplifier, Large and small signal analysis of the balanced differential amplifier, device mismatches in differential amplifier, small and large signal analysis of the differential pair with current mirror load, $PSRR^+$, $PSRR^-$ and CMRR of differential amplifiers, small signal analysis of telescopic amplifier, two-stage amplifier and folded cascaded amplifier.

MODULE IV FREQUENCY RESPONSE OF MULTISTAGE DIFFERENTIAL AMPLIFIERS 6L

Dominant-Pole approximation, zero-value time constant analysis, - Frequency response of current mirror loaded, differential amplifier, short circuit time constants, frequency response of telescopic cascaded, folded cascode amplifier.

MODULE V STABILITY AND FREQUENCY COMPENSATION OF FEEDBACK AMPLIFIERS 8L

Properties and types of negative feedback circuits, feedback configurations, effect of loading in feedback networks, feedback circuit analysis using return ratio- modelling input and output port in feedback network, the relation between gain and bandwidth in feedback amplifiers, phase margin, frequency compensation, compensation of two stage MOS amplifiers.

TOTAL:36 PERIODS

REFERENCES:

1. Gray, Hurst, Lewis, Meyar, “Analysis and Design of Analog Integrated Circuits” John

Wiley, 5th Edition, 2009.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Twelfth Reprint, Tata Mc Graw Hill, 2012.
3. Phillip E. Allen, Douglas R.Holberg, "CMOS Analog Circuit Design", Oxford University Press, 3rd Edition, 2011.
4. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation", Wiley IEEE Press, 3rd Edition, 2010.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	3	2	-	-	3	2
CO2	3	3	3	2	-	3	2
CO3	3	3	3	3	-	3	3
CO4	3	3	2	2	-	3	3

Paper Code: ADVANCED DIGITAL SYSTEM DESIGN
Paper Code: MEC102
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

At the end of the course, the student should be able to:

CO1 Analyze and design synchronous sequential circuits using state diagrams, state tables, and Algorithmic State Machine (ASM) charts.

CO2 Design asynchronous sequential circuits by handling flow table reduction, race conditions, and various types of hazards.

CO3 Apply fault diagnosis and testability algorithms such as D-algorithm, Boolean difference method, and BIST techniques to evaluate sequential circuit reliability.

CO4 Implement synchronous designs using programmable logic devices (PLDs), including PLA, PAL, and FPGA-based finite state machines.

CO5 Develop Verilog HDL models for combinational and sequential circuits, and synthesize and simulate hardware systems such as counters, FSMs, and simple processors.

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MODULE I: SEQUENTIAL CIRCUIT DESIGN 6L

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

MODULE II:ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 8L

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

MODULE III: FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 6L

Fault table method-path sensitization method – Boolean difference method-D algorithm -

Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

MODULE IV: SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 8L

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

MODULE V : SYSTEM DESIGN USING VERILOG 8L

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

TOTAL:36 PERIODS

REFERENCES:

1. Charles H.Roth Jr "Fundamentals of Logic Design", Thomson Learning, 2004.
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.
3. M.G.Arnold, "Verilog Digital – Computer Design", Prentice Hall (PTR), 1999.
4. Nripendra N Biswas "Logic Design Theory", Prentice Hall of India,2001.
5. Parag K.Lala "Digital system Design using PLD", B S Publications, 2003.
6. Parag K.Lala "Fault Tolerant and Fault Testable Hardware Design", B S Publications,2002.
7. S. Palnitkar , "Verilog HDL – A Guide to Digital Design and Synthesis", Pearson , 2003.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	3	2	2	–	3	2
CO2	3	3	2	2	–	3	2
CO3	3	3	2	3	–	3	3
CO4	3	2	3	2	–	3	2
CO5	3	2	3	3	1	3	3

Paper Code: SEMICONDUCTOR DEVICES
Paper Code: MEC103A
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

At the end of the course the student will be able to:

CO1- Understand the physical behavior of semiconductor devices. (Cognitive-Understanding)

CO2- Identify challenges of scaling in semiconductor devices. (Cognitive- Applying)

CO3- Compare performance metrics of semiconductor devices at different technology node. (Skills- Evaluate)

CO4- Design and Optimization of device for low power and high-performance circuits.

(Affective- Create)

MODULE I BASIC SEMICONDUCTOR PHYSICS **7L**

Crystal lattice, energy band model, density of states, distribution statics – Maxwell-Boltzmann and Fermi-Dirac, doping, carrier transport mechanisms, drift, diffusion, thermionic emission, and tunneling; excess carriers, carrier lifetime, recombination mechanisms – SHR, Auger.

MODULE II P-N JUNCTION AND METAL-SEMICONDUCTOR JUNCTION **8L**

P-N junctions- fabrication, basic operation – forward and reverse bias, DC model, charge control model, I-V characteristics, steady-state and transient conditions, capacitance model, reverse-bias breakdown, SPICE model; metal-semiconductor junctions –fabrication, Schottky barriers, rectifying and ohmic contacts, I-V characteristics.

MODULE III MOS CAPACITORS AND MOSFETS **8L**

The MOS capacitor – fabrication, surface charge, accumulation, depletion, inversion, threshold voltage, C-V characteristics – low and high frequency; MOSFET – fabrication, operation, gradual channel approximation, simple charge control model (SCCM), Pao-Sah and Schichman – Hodges models, I- V characteristics, second-order effects – Velocity saturation, short-channel effects, charge sharing model, hot-carrier effects, gate tunneling; subthreshold operation – drain induced barrier lowering (DIBL) effect, unified charge control model(UCCM), SPICE level 1, 2, and 3, and Berkeley short-channel model (BSIM).

MODULE IV MESFET AND HEMTS **7L**

Fabrication, basic operation, Shockley and velocity saturation models, I-V characteristics, high-frequency response, back gating effect, SPICE model; HEMTs – fabrication, modulation (delta) doping, analysis of III-V heterojunctions, charge control, I-V characteristics, SPICE model.

MODULE V ADVANCED MOSFET TECHNOLOGY **6L**

Partially and fully depleted SOI MOSFETs, high-k MOS devices, strained technology, metal gate electrode, FinFETs and Multi gate MOSFETs, enhanced quasi ballistic transport, Si Nanowire MOSFETs.

TOTAL:36 PERIODS

REFERENCES:

1. Physics of Semiconductor Devices: *S. M. Sze, Wiley Eastern, (1981).*
2. Semiconductor physics and Devices, Donald Neamen, McGraw-Hill, 3rd edition.
3. Solid State Electronic Devices, B.G.Streetman and S.Banerjee, Prentice Hall India.
4. CMOS Circuit Design, Layout and simulation: *J. Baker, D.E. Boyce., IEEE press*.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	3	1	-	-	3	2
CO2	3	3	2	2	-	3	3
CO3	3	3	2	3	-	3	3
CO4	3	3	3	3	2	3	3

Paper Code: VLSI PROCESS TECHNOLOGY
Paper Code: MEC103B
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

CO1 Understand the major steps in the fabrication process of VLSI circuits.

CO2 Illustrate particular processing steps in achieving required parameters.

CO3 Apply standard engineering for different lithographic methods.

CO4 Analyse the specific plasma process used in semiconductor industry

CO5 Apply implantation process for VLSI devices and discuss the limitations of various metallization schemes.

MODULE I: CRYSTAL GROWTH AND WAFER PREPARATION **6L**

Introduction, Electronic-Grade Silicon, Czochralski Crystal Growing.

MODULE II: EPITAXY **6L**

Introduction, Vapour-Phase Epitaxy.

MODULE III: LITHOGRAPHY: **6L**

Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography.

MODULE IV: REACTIVE PLASMA ETCHING: **6L**

Introduction, Plasma Properties, Feature-Size Control and Anisotropic Etch Mechanisms, Other Properties of Etch Processes, Reactive Plasma-Etching Techniques and Equipment, Specific Etch Processes.

MODULE V: ION IMPLANTATION **6L**

Introduction, Range Theory, Implantation Equipment, Annealing, Shallow Junctions, High-Energy Implantation.

MODULE VI: METALLIZATION **6L**

Introduction, Metallization Applications, Metallization Choices, Physical Vapor Deposition, Patterning, Metallization problems.

TOTAL:36 PERIODS

REFERENCES:

1. S. M. Sze, **"VLSI Technology"**, McGraw-Hill, Second Edition.
2. S.K. Ghandhi, **"VLSI Fabrication Principles"**, John Wiley Inc., New York, 1994, Second Edition.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	2	–	–	–	3	2
CO2	3	2	–	2	–	3	2
CO3	3	3	2	2	–	3	2
CO4	3	3	2	2	–	3	3
CO5	3	3	2	2	–	3	3

Paper Code: COMPUTER AIDED DESIGN OF DIGITAL SYSTEM
Paper Code: MEC103C
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

CO1 Understand various VLSI design domains, design actions, and technologies used in different design methodologies.

CO2 Apply algorithmic and system-level approaches to VLSI design automation using concepts of graph theory and computational complexity.

CO3 Compare schematic-level and layout-level design problems and apply combinatorial optimization techniques for layout compaction.

CO4 Demonstrate knowledge of VLSI physical design stages including placement, partitioning, floorplanning, and routing strategies.

CO5 Analyze various levels of simulation and synthesis in VLSI, including gate-level, switch-level, and high-level modeling and verification techniques.

MODULE I: INTRODUCTION TO VLSI METHODOLOGIES **6L**

Design domains and actions. Design methods and technologies.

MODULE II: VLSI DESIGN AUTOMATION TOOLS **8L**

Structural and transistor level design algorithmic and system design algorithmic graph theory and computational complexities

MODULE III:SCHEMATIC VS LAYOUT **6L**

Tractable and intractable problems, general purpose methods for combinational optimization, Layout compaction

MODULE IV: LAYOUT **8L**

Placement and partitioning, Floor planning concepts, Routing definition and Concept

MODULE V: SIMULATION **8L**

Simulation – general remarks on VLSI simulation, gate level modelling and simulation switch level modeling and simulation logic synthesis and verification, high level synthesis

TOTAL:36 PERIODS

REFERENCES:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", 1998
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", 1999
3. JA Bondy, USR Murty "Graph Theory With Applications" Elsevier Science Publishing Co. Inc , 1982
4. Giovanni De Micheli ,"Synthesis And Optimization Of Digital Circuits".

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	2	2	–	–	3	2
CO2	3	3	2	2	–	3	3
CO3	3	3	2	2	–	3	3
CO4	3	2	3	2	–	3	2
CO5	3	2	3	3	–	3	3

Paper Code: MEMS AND MICROSYSTEMS
Paper Code: MEC104A
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

CO1 Understand the fundamental concepts of MEMS and Microsystems, including microfabrication techniques, sensors, actuators, and material selection.

CO2 Analyze mechanical properties and micromechanics such as stress, strain, bending, vibration, and thermomechanical behavior in MEMS structures.

CO3 Design electrostatic and electromagnetic microactuators by applying principles of electrostatics, surface tension, and actuator dynamics.

CO4 Evaluate electronic interfacing, noise issues, and packaging techniques for MEMS integration including wafer-level and self-assembly methods.

CO5 Analyze system-level design and performance of RF and Optical MEMS through real-world case studies like accelerometers, sensors, and MEMS switches.

MODULE I: INTRODUCTION TO MEMS **8L**

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication

MODULE II: MICROMECHANICS **8L**

Elasticity, Stress, strain and material properties, Bending of thin films, Spring configurations, torsion deflection, Mechanical vibration, Resonance, Thermomechanics - actuators, force and response time, Fracture and thin film mechanics.

MODULE III: MICROACTUATORS **8L**

Electrostatics: basic theory, electrostatic instability. Surface tension, Gap and finger pull up, Electrostatic actuators, comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators, bistable actuators.

MODULE IV: INTERFACING AND PACKAGING **6L**

Electronic Interfaces, Feedback systems, Noise, Packaging: Dicing-Wafer level Packaging-Wafer bonding-Connections between layers-self assembly-higher level of packaging.

MODULE V: CASE STUDIES **6L**

Optical MEMS, RF MEMS- System design basics, Case studies: Capacitive accelerometer, Peizo electric pressure sensor, MEMS scanners, Capacitive RF MEMS switch, performance issues.

TOTAL:36 PERIODS

REFERENCES:

1. Stephen D Senturia, "Microsystems Design", Springer Publishers, 2nd Edition, 2005.
2. Nadim Maluf and Kirt Williams, "Introduction to Microelectromechanical Systems Engineering", Artech House, 2004.
3. Mohamed Gad-el-Hak, Editor, "The MEMS Handbook", CRC press, 2nd Edition, 2005.
4. Tai - Ran Hsu, "MEMS and Micro Systems: Design, Manufacture and Nanoscale Engineering", Tata McGraw Hill, New Delhi, 2nd Edition, 2008.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	2	2	–	–	3	2
CO2	3	3	–	2	–	3	3
CO3	3	3	2	2	–	3	3
CO4	3	2	2	2	1	3	2
CO5	3	3	3	2	1	3	3

Paper Code: SOFTWARE FOR EMBEDDED SYSTEMS
Paper Code: MEC104B
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

- To understand basic concepts of Embedded Systems.
- To know development of Hardware Software co-design in Embedded System.
- To understand Architecture of ARM-32 bit Microcontroller.
- To analyse Instruction sets by Assembly basics, Instruction list and description.
- To learn Cortex-M3 programming using C language concepts and Microcontroller Software Interface Standard concepts.

MODULE I: INTRODUCTION TO EMBEDDED SYSTEMS 6L

Overview of Embedded Systems ,Characteristics and Constraints, Embedded Hardware Overview (Microcontrollers, DSPs, FPGAs, ASICs), Applications of Embedded Systems, Embedded System Development Life Cycle.

MODULE II: EMBEDDED PROGRAMMING AND DEVELOPMENT ENVIRONMENTS 8L

Programming Languages for Embedded Systems (C, C++, Assembly), Embedded Software Development Tools, Cross-compilers and Linkers, Debugging Tools (JTAG, GDB, Trace Tools), IDEs and Simulators, Software Development Process for Embedded Systems, Embedded C vs. Standard C

MODULE III: REAL-TIME OPERATING SYSTEMS (RTOS) 8L

Basics of Real-Time Systems, Concepts of Tasks, Threads, and Processes, Scheduling in RTOS (Preemptive, Cooperative, Round-Robin, Priority-based Scheduling), Interprocess Communication (Semaphores, Mutexes, Message Queues), RTOS Examples (FreeRTOS, VxWorks, uC/OS), Task Synchronization and Deadlocks

MODULE IV: EMBEDDED COMMUNICATION AND NETWORKING 6L

Serial Communication Protocols (UART, SPI, I2C), Wireless Communication (Wi-Fi, Bluetooth, Zigbee), Real-Time Networking Protocols (CAN, LIN, MODBUS), TCP/IP Stack in Embedded Systems, Embedded Web Servers

MODULE V: EMBEDDED SOFTWARE TESTING AND DEBUGGING 8L

Testing Strategies for Embedded Software, Unit Testing and Integration Testing in Embedded Systems, Code Coverage and Static Analysis Tools, Debugging Techniques (Hardware Debuggers, Logic Analyzers, Oscilloscopes), Case Study: Debugging an Embedded System

TOTAL:36 PERIODS

REFERENCES:

1. Raj Kamal, "Embedded Systems- Architecture, Programming and Design", Tata Mc Graw-Hill Publications, 2nd Edition, 2008.
2. John Davies, "MSP 430 Microcontroller Basics", Elsevier, 2008.
3. YifengZhu, “Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C**”,** E-Man Press LLC, 1st Edition, 2014.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	2	–	–	–	3	2
CO2	3	2	2	2	–	3	2
CO3	3	2	–	–	–	3	2
CO4	3	2	–	–	–	3	2
CO5	3	2	3	2	1	3	3

Paper Code: DISTRIBUTED EMBEDDED COMPUTING
Paper Code: MEC104C
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

- To expose the students to the fundamentals of Network communication technologies.
- To teach the fundamentals of Internet
- To study on Java based Networking
- To introduce network routing Agents
- To study the basis for network on-chip technologies

MODULE I: THE HARDWARE INFRASTRUCTURE 8L

Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.

MODULE II: INTERNET CONCEPTS 6L

Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

MODULE III: DISTRIBUTED COMPUTING USING JAVA 8L

IO streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.

MODULE IV: EMBEDDED AGENT 6L

Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

MODULE V: EMBEDDED COMPUTING ARCHITECTURE 8L

Synthesis of the information technologies of distributed embedded systems – analog/digital co- design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.

TOTAL:36 PERIODS

REFERENCES:

1. Dietel & Dietel, “JAVA how to program”, Prentice Hall, 1999.
2. Sape Mullender, “Distributed Systems”, Addison-Wesley, 1993.
3. George Coulouris and Jean Dollimore, “Distributed Systems – concepts and design”,Addison –Wesley, 1988.
4. “Architecture and Design of Distributed Embedded Systems”,Bernd Kleinjohann C- lab, Universitat Paderborn, Germany, Kluwer Academic Publishers, Boston, 2001.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	2	–	–	–	3	2
CO2	3	2	2	–	–	3	2
CO3	3	3	3	2	1	3	3
CO4	3	3	2	2	2	3	3
CO5	3	3	3	3	–	3	3

Paper Code: RESEARCH METHODOLOGY AND IPR
Paper Code: MLC101
Contact hours: 36
Credits: 3

COURSE OUTCOMES: At the end of this course, students will be able to

CO1: Solve research problem formulation.
CO2: Analyze research related information
CO3: Maintain research ethics
CO4: Convince new incumbents that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
CO5: Realize that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
CO6: Demonstrate that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

MODULE I: Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations. **6L**

MODULE II: Effective literature studies approaches, analysis Plagiarism, Research ethics**. 6**

MODULE III: Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee. **6L**

MODULE IV: Nature of Intellectual Property: Patents, Designs, Trademarks and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT. **6L**

MODULE V: Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and data bases. Geographical Indications**. 6L**

MODULE VI: New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs. **6L**

TOTAL:36 PERIODS

REFERENCES:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
5. Mayall , "Industrial Design", McGraw Hill, 1992.
6. Niebel , "Product Design", McGraw Hill, 1974.
7. Asimov , "Introduction to Design", Prentice Hall, 1962.
8. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
9. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	3	1	2	-	2	3
CO2	3	3	2	3	-	2	3
CO3	3	3	1	-	3	2	3
CO4	2	2	1	-	3	2	3
CO5	3	2	1	-	3	3	3
CO6	3	2	1	-	3	3	3

Paper Code: FPGA SYSTEM DESIGN LABORATORY
Paper Code: MEC191
Contact hours: 36
Credits: 2

COURSE OUTCOMES:

At the end of the course, the student should be able to
CO1: Write HDL codes for digital circuits satisfying given specification.
CO2: Import the logic modules into FPGA Boards.
CO3: Synthesis, Place and Route the digital IPs.
CO4: Use FPGA EDA tools for design and analysis.

EXPERIMENTS:

1. Design Entry Using VHDL or Verilog using HDL languages of
   i. Combinational circuits namely 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder.
   ii. Sequential circuits namely D-FF, 4-bit Shift registers (SISO, SIPO,

PISO, bidirectional), 3-bit Synchronous Counters.

2. Test vector generation and timing analysis of sequential and combinational logic design in (1).
3. Synthesis, P&R and post P&R simulation of the components simulated in (1) above. Critical paths to be identified. Identify and verify possible conditions under which the blocks will fail to work correctly.
4. FPGA implementation of PCI Bus & arbiter.
5. Interfacing with Memory modules in FPGA Boards.
6. Realization of Discrete Fourier transform/Fast Fourier Transform algorithm in HDL and observing the spectrum in simulation.
7. Verification of design functionality implemented in FPGA by capturing the signal in DSO.
8. Verifying design functionality using either chipscope feature (Xilinx) /the signal tap feature (Altera)/other equivalent feature. Invoke the PLL and demonstrate the use of the PLL module for clock generation in FPGAs.

TOTAL:36 PERIODS

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	3	3	2	-	3	3
CO2	3	3	3	2	-	3	3
CO3	3	3	3	2	-	3	3
CO4	3	3	3	3	-	3	3

Paper Code: ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY
Paper Code: MEC192
Contact hours: 36
Credits: 2

COURSE OUTCOMES:

- To understand the various analog and digital circuits and their simulation using Cadence tool.
- To learn the advanced concepts of modern VLSI circuit and system design
- To design common sequential functions: flip-flops, registers, latches, and state-machines.
- To understand placement, routing, and verify timing of a standard cell design.

ANALOG IC DESIGN (USING SPICE CIRCUIT SIMULATION TOOL):

Circuit simulation, Layout generation, parasitic extraction, Synthesis and Standard cell based design of the circuits. Identification of critical paths, power consumption. P&R, power and clock routing, post P&R simulation and Static timing analysis of:

1. Design of CMOS Inverter - Circuit Simulation, transfer characteristic curve, transient analysis, Layout design.

2. Design of Current Mirrors - Simple current source generator, Current mirror, Wilson Current mirror circuit, Layout of the current mirror circuit.

3. A simple differential amplifier. Measure gain, ICMR, and CMRR - Differential input, single ended differential amplifier design, Differential amplifier design, telescopic amplifier design, layout of differential amplifier.

DIGITAL DESIGN (HDL Design Entry Tool):

1. HDL based design entry and simulation of Parameterizable cores of Counters, Shift registers, State machines, 8-bit Parallel adders and 8 –Bit multipliers.

2. HDL based design entry and simulation of Parameterizable cores on the simple Distributed Arithmetic system.

3. HDL based design entry and simulation of Parameterizable cores on memory design and 4 – bit ALU.

4. Synthesis, P&R and post P&R simulation, Critical paths and static timing analysis results to be identified.

5. Timing Analysis by using EDA TOOLs

a) Static Timing Analysis (STA) of a Digital Circuit Using an EDA Tool(Synopsis).

b) Setup and Hold Time Violation Analysis and Timing Optimization Using EDA Tools(Synopsis).

TOTAL:36 PERIODS

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	2	3	2	–	3	2
CO2	3	2	3	2	–	3	3
CO3	3	3	2	2	1	3	2
CO4	3	3	3	3	–	3	3

SEMESTER II

Paper Code: SoC DESIGN FOR EMBEDDED SYSTEM
Paper Code: MEC201
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

CO1 Understand the architecture, design complexity, and trade-offs involved in developing a System-on-Chip (SoC).

CO2 Analyze processor architectures, instruction handling, and selection strategies for designing robust and efficient SoC processors.

CO3 Design efficient memory systems for SoCs, including cache architecture, memory hierarchies, and interaction between processors and memory.

CO4 Evaluate interconnect architectures and apply SoC customization techniques using reconfigurable platforms like FPGAs.

CO5 Implement hardware/software co-design principles in FPGA-based embedded processors, including interface design and custom microcontroller development.

MODULE I SYSTEM ARCHITECTURE: OVERVIEW 7L

Components of the system – Processor architectures – Memory and addressing – system level interconnection — SoC design requirements and specifications — design integration — design complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability.

MODULE II PROCESSOR SELECTION FOR SOC 8L

Overview – soft processors, processor core selection. Basic concepts – instruction set, branches, interrupts and exceptions. Basic elements in instruction handling – Minimizing pipeline delays – reducing the cost of branches — Robust processors — Vector processors, VLIW processors, Superscalar processors.

MODULE III MEMORY DESIGN 7L

SoC external memory, SoC internal memory, Scratch pads and cache memory — cache organization and write policies — strategies for line replacement at miss time — split I- and D- caches — multilevel caches — SoC memory systems — board based memory systems — simple processor/memory interaction.

MODULE IV INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION 6L

Bus architectures — SoC standard buses — AMBA, CoreConnect — Processor customization approaches — Reconfigurable technologies — mapping designs onto reconfigurable devices - FPGA based design – Architecture of FPGA, FPGA interconnect technology, FPGA memory, Floor plan and routing.

MODULE V FPGA BASED EMBEDDED PROCESSOR 8L

Hardware software task partitioning – FPGA fabric Immersed Processors – Soft Processors and Hard Processors — Tool flow for Hardware/Software Co-design –Interfacing Processor with memory and peripherals — Types of On-chip interfaces — Wishbone interface, Avalon Switch Matrix, OPB Bus Interface, Creating a Customized Microcontroller - FPGA-based Signal Interfacing and Conditioning.

TOTAL:36 PERIODS

REFERENCES:

1. Michael J. Flynn and Wayne Luk**,** "Computer System Design: System-on-Chip", John Wiley and sons, 2011.
2. Rahul Dubey, "Introduction to Embedded System Design Using Field Programmable Gate Arrays", Springer Verlag London Ltd., 2009.
3. Sudeep Pasricha and Nikil Dutt, On-Chip Communication Architectures - System on Chip Interconnect, Elsevier, 2008.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	2	2	2	–	3	3
CO2	3	3	2	2	–	3	3
CO3	3	3	3	2	–	3	3
CO4	3	2	3	2	–	3	3
CO5	3	3	3	3	1	3	3

Paper Name: VLSI SIGNAL PROCESSING
Paper Code: MEC202
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

CO1 Analyze DSP algorithms using data flow and dependence graphs and apply pipelining and parallel processing techniques to optimize digital filter design.

CO2 Apply algorithmic strength reduction techniques such as retiming and unfolding for efficient VLSI implementation of DSP architectures.

CO3 Design optimized recursive and non-recursive DSP systems using fast convolution algorithms and look-ahead pipelining methods.

CO4 Develop efficient bit-level arithmetic architectures including serial and parallel multipliers, FIR filters, and distributed arithmetic-based implementations.

CO5 Evaluate numerical strength reduction techniques and advanced pipelining strategies like wave and asynchronous pipelining for high-performance VLSI design.

MODULE I PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS 7L

Introduction to DSP systems — Typical DSP algorithms, Data flow and Dependence graphs — critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

MODULE II ALGORITHMIC STRENGTH REDUCTION TECHNIQUE - I 7L

Retiming — definitions and properties, Unfolding — an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

MODULE III ALGORITHIMIC STRENGTH REDUCTION -II 8L

Fast convolution — Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters — Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

MODULE IV BIT-LEVEL ARITHMETIC ARCHITECTURES **8L**

Bit-level arithmetic architectures — parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

MODULE V NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING **6L**

Numerical strength reduction — subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL:36 PERIODS

REFERENCES:

1. Keshab K. Parhi, "V L S I Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, 2nd Edition, 2004.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	3	2	2	–	3	3
CO2	3	3	2	2	–	3	3
CO3	3	3	2	3	–	3	3
CO4	3	3	3	2	–	3	3
CO5	3	3	3	3	–	3	3

Paper Code: VLSI TESTING AND VERIFICATION
Paper Code: MEC203A
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

- To know the various types of faults in VLSI based digital circuits.
- To examine various techniques available for efficient fault detection in combinational circuits.
- To learn the techniques to enhance testability of combinational circuits.
- To learn various techniques that can be used to make sequential circuits easily testable.
- To understand test generation and response evaluation techniques used in BIST schemes for VLSI Chips

MODULE I FAULTS IN DIGITAL CIRCUITS **8L**

Failures and Faults, Modeling of faults, Temporary Faults. **Logic Simulation**: Applications, Problems in simulation based design verification, types of simulation, The unknown logic

values, compiled simulation, event-driven simulation, Delay models, Element evaluation, Hazard Detection, Gate-level event-driven Simulation

MODULE II TEST GENERATION FOR COMBINATIONAL LOGIC CIRCUITS 7L

Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational logic circuits.

MODULE III TESTABLE COMBINATIONAL LOGIC CIRCUIT DESIGN 7L

Testable design of multilevel combinational circuits, Synthesis of random pattern testable combinational circuits, Path delay fault testable combinational logic design, Testable PLA design.

MODULE IV DESIGN OF TESTABLE SEQUENTIAL CIRCUITS 8L

Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable sequential circuit design, Level Sensitive Scan Design (LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Non scan Techniques, Cross check, Boundary Scan.

MODULE V BUILT-IN SELF TEST 6L

Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures.

TOTAL:36 PERIODS

REFERENCES:

1. P. K. Lala, **"Digital Circuit Testing and Testability"**, Academic Press
2. M.L. Bushnell and V.D. Agrawal, **"Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits"**, Kluwar Academic Publishers.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, **"Digital Systems and Testable Design"**, Jaico Publishing House, 2002.
4. Janick Bergeron, **"Writing test benches: functional verification of HDL models"**, 2nd edition ,Kluwer Academic Publishers,2003
5. Jayaram Bhasker, Rakesh Chadha ,**"Static Timing Analysis for Nanometer Designs"** A practical approach, Springer publications
6. Prakash Rashinkar, Peter Paterson, Leena Singh **"System on a Chip Verification"**, Kulwer Publications.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	3	1	-	-	3	2
CO2	3	3	2	2	-	3	3
CO3	3	3	2	2	-	3	3
CO4	3	3	2	2	-	3	3
CO5	3	3	1	2	-	3	3

Paper Code: LOW POWER VLSI DESIGN
Paper Code: MEC203B
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

CO1 Identify the sources of power dissipation in CMOS circuits.
CO2 Perform power analysis using simulation-based approaches and probabilistic analysis.
CO3 Use optimization and trade-off techniques that involve power dissipation of digital circuits.
CO4 Make the power design a reality by making power dimension an integral part of the design process.
CO5 Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.

MODULE I: **INTRODUCTION** **8L**

Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits.

Simulation power analysis: SPICE circuit simulation, Monte Carlo simulation.

MODULE II: SCHEMATIC CIRCUIT DESIGN TECHNIQUES **6L**

Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage.

MODULE III: LOGICAL DESIGN **8L**

Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers.

MODULE IV: **LOW POWER ARCHITECTURE & SYSTEMS** **8L**

Power & performance management, switching activity reduction, flow graph transformation.

Low power memory design: Introduction, sources and reductions of power dissipation in memory subsystem.

MODULE V: **ALGORITHM & ARCHITECTURAL LEVEL METHODOLOGIES**: **6L**

Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Advanced Techniques: Adiabatic computation, Asynchronous circuits.

TOTAL:36 PERIODS

REFERENCES:

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic, 1998.
2. Jan M. Rabaey, Massoud Pedram, "Low Power Design Methodologies", Kluwer Academic, 2010.
3. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000
4. A. P. Chandrasekaran and R. W. Broadersen, "Low power digital CMOS design", Kluwer Academic,1995.
5. A Bellamour and M I Elmasri, "Low power VLSI CMOS circuit design", Kluwer Academic,1995.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	2	–	–	–	3	2
CO2	3	3	2	3	–	3	3
CO3	3	3	3	2	–	3	3
CO4	3	3	3	2	–	3	3
CO5	3	3	3	2	–	3	3

Paper Code: DIGITAL SYSTEM DESIGN & FPGAS
Paper Code: MEC203C
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

CO1: To be able to apply the basic design principles of sequential logic systems. (Cognitive- Applying)
CO2: To understand the design concepts of synchronous state machines in Moore and Mealy architectures. (Cognitive- understanding)
CO3: To analyze & design data path, control path design and various programmable devices (Skills- Create)
CO4: To be able to implement a digital system using HDLs (Skills- Evaluate)

MODULE I SEQUENTIAL LOGIC DESIGN **7L**

Introduction, Basic Bistable Memory Devices, additional bistable devices, reduced characteristics an excitation table for bistable devices.

MODULE II SYNCHRONOUS SEQUENTIAL LOGIC CIRCUIT DESIGN **8L**

Introduction, Moore, Mealy and Mixed type Synchronous State Machines. Synchronous sequential design of Moore, Melay Machines,

MODULE III ALGORITHMIC STATE MACHINE **7L**

ASM Chart Representation, Implementation of traffic light controller, Applications of ASM, Design Procedure for ASMs.

MODULE IV DATA PATH AND CONTROL DESIGN. **6L**

Components of Data Path, Design Considerations, Components of Control Path, Design

Considerations, Integration of Data Path & Control Path, ALU Operation in a Processor, Optimization Techniques

MODULE V INTRODUCTION TO VHDL/VERILOG **8L**

Data types, Concurrent statements, sequential statements, behavioral modeling. Introduction to programmable logic devices- PALs, PLDs, CPLDs and FPGAs.

TOTAL:36 PERIODS

REFERENCES:

1. Digital System Design, Ercegovac, Wiley.
2. Richard S. Sandige, *Modern Digital Design,* McGraw-Hill, 1990.
3. Zvi Kohavi, Switching and Finite Automata Theory, Tata McGraw-Hill.
4. Navabi. Analysis and modeling of digital systems. McGraw Hill, 1998.
5. Perry. Modeling with VHDL. McGraw Hill, 1994.
6. Navabi. Verilog Digital Design. McGraw Hill, 2007.
7. Fundamentals of Digital Logic with Verilog Design, Stephen Brown and Zvonko Vranesic, McGraw Hill, 2002.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	3	2	-	-	3	2
CO2	3	3	1	-	-	3	2
CO3	3	3	3	2	-	3	3
CO4	3	3	3	3	2	3	3

Paper Code: ADVANCED EMBEDDED SYSTEMS
Paper Code: MEC204A
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

CO1 Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.

CO2 Explain the hardware software co-design and firmware design approaches.

CO3 Understand the suitability of the instruction sets of ARM processors to design of embedded systems.

CO4 Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32-bit microcontroller including memory map, interrupts and exceptions.

CO5 Apply the knowledge gained for Programming ARM CORTEX M3 for different applications

MODULE-I EMBEDDED SYSTEM: **6 L**

Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems

MODULE -II EMBEDDED SYSTEM HARDWARE: 10L

Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), simulators, emulators and debugging

MODULE -III ARM-32 BIT MICROCONTROLLER: 8L

Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence.

MODULE -IV INSTRUCTION SETS: 6L

Assembly basics, Instruction list and description, useful instructions, Memory maps, Memory access attributes, Default Memory Access Permissions, Bit band operations, Endian Mode.

MODULE -V INTERRUPTS: 6L

Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS.

TOTAL:36 PERIODS

REFERENCES:

1. K. V. Shibu , "Introduction to embedded systems", TMH education Pvt. Ltd. 2009
2. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier) 2nd edn, 2010.
3. James K. Peckol , "Embedded systems - A contemporary design tool", John Wiley, 2008

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	2	2	1	–	3	1
CO2	2	3	2	1	1	3	2
CO3	2	3	3	–	–	3	2
CO4	2	2	3	–	–	3	2
CO5	2	3	3	2	1	3	3

Paper Code: INTRODUCTION TO EMBEDDED CONTROLLERS
Paper Code: MEC204B
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

- To learn about the designing of an embedded system for commercial applications.
- To learn the features, architecture and programming of PIC and ARM microcontrollers
- To study the interfacing peripherals with microcontrollers.

- To learn about the communication protocols in a Microcomputer system.
- To learn about the fundamentals of real-time operating system in an embedded system.

MODULE I INTRODUCTION TO EMBEDDED SYSTEMS 8L

Processor Embedded into a System, Embedded Hardware Units and Devices in a System, Embedded Software in a System, Examples of Embedded Systems, Embeded System on-chip (Soc) and Use of VLSI Circuit Design Technology, Complex Systems Design and Processors, Design Process in Embedded Systems, Formalization of System Design, Design Process and Design Examples, Classification of Embedded Systems.

MODULE II ATMEGA MICROCONTROLLERS 7L

Architecture, Features, Memory and memory map, I/O ports, Timers and CCP Devices, ADC, Interrupts, Instruction format, Addressing Modes, Instruction Set, Programming with MPLAB IDE.

MODULE III 16 BIT MICROCONTROLLER 7L

Introduction to 16 bit Processors, MSP430 - RISC CPU Architecture - Compiler friendly features - Instruction sets - Clock System - Memory Subsystem - Bus Architecture, different families in MSP 430 (2xx,4xx,5xx,6xx) - Key differentiating factors between families.

MODULE IV INTERFACING I/O DEVICES AND COMMUNICATION PROTOCOLS 8L

LED, liquid crystal display, Motor (DC, Servo, Stepper), Relays, Keypad, Keyboard, Touch screen, Sensors (thermocouple, force, displacement), SD card, Infrared connectivity, Serial communication protocols (UART, I2C, SPI, CAN, USB, LIN), Parallel communication protocols (PCI, ISA), Wireless communication networks (Bluetooth, Zigbee, Wifi, GSM), Global positioning system receivers, Embedded Systems and the internet.

MODULE V MULTITASKING AND THE REAL-TIME OPERATING SYSTEM 6L

The challenges of multitasking and real-time, Achieving multitasking with sequential programming, RTOS, Scheduling and the scheduler, Developing tasks, Data and resource protection- the semaphore, Examples using Salvo Real-time operating systems.

TOTAL:36 PERIODS

REFERENCES:

1. Raj Kamal, "Embedded Systems- Architecture, Programming and Design", Tata Mc Graw-Hill Publications, 2nd Edition, 2008.
2. John Davies, "MSP 430 Microcontroller Basics", Elsevier, 2008.
3. YifengZhu, “Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C**”,** E-Man Press LLC, 1st Edition, 2014.
4. Tim Wilmshurst, "Designing Embedded Systems with PIC Microcontrollers- Principles and Applications", Newnes Publications, 2007.
5. Julio Sanchez Maria P.Canton, “Microcontroller Programming: The microchip PIC”, CRC Press, Taylor & Francis Group,2007.
6. Thomas Grace, **“**Programming and Interfacing Atmel AVR Microcontrollers”, Cengage Learning PTR, 2015.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	3	1	-	-	3	2
CO2	3	3	2	-	-	3	2
CO3	3	3	3	2	-	3	3
CO4	3	3	2	-	-	3	2
CO5	3	3	2	2	-	3	3

Paper Code: Embedded Programming
Paper Code: MEC204C
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

CO1: Apply C and Embedded C concepts for embedded system programming.
CO2: Use Linux commands, shell scripting, and file management techniques effectively.
CO3: Implement kernel data structures and understand kernel architecture.
CO4: Develop and compile Linux kernel modules.
CO5: Design and implement basic character device drivers.

Module I: Fundamentals of C (7L)

Basic concepts of C; Embedded C vs C; Embedded programming aspects with respect to firmware and OS functions; Arrays; Pointers; Structures; Input/Output operations.

Module II: Data Structures of Kernel Programming (6L)

Linked list; Single linked list; Double linked list; Queues.

Module III: Basics of Linux (6L)

Command prompt; X Windows basics; Navigating file system; Finding files; Working with folders; Reading files; Text editing in Linux; Compression and archiving tools; Basic shell commands; File management; Input/Output handling; File locking.

Module IV: Shell Programming (7L)

Processes; Executing more than one command at a time; Prioritizing processes; Killing processes; Scheduling commands; Pipes and redirection; Regular expressions; Pattern matching; Scripting using for, while, if and other commands.

Module V: Basics of Embedded Linux (6L)

Linux basics; Booting process; Makefiles; Using SD card and reader to transfer programs; Introduction to Linux system calls; APIs; Device drivers; Compiling and installing a device driver.

Module VI: Kernel Module Programming (6L)

Compiling kernel; Configuring kernel and compilation; Kernel code browsers; Static linking; Dynamic linking of modules; User space and kernel space concepts; Writing simple modules; Writing Makefiles for modules.

Module VII: Device Driver Basics (5L)

Driver concepts; Block and character driver distinction; Low-level drivers; OS drivers; Writing character drivers; Device major and minor numbers.

Reference Books

1. W. Richard Stevens and Stephen Rago, Advanced Programming in the UNIX Environment, Addison-Wesley.
2. Daniel P. Bovet and Marco Cesati, Understanding the Linux Kernel, O'Reilly.
3. Karim Yaghmour, Building Embedded Linux Systems, O'Reilly.

COs	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	2	2	-	2	3	2
CO2	2	3	2	-	3	3	2
CO3	3	3	2	2	2	3	3
CO4	3	2	3	2	3	3	2
CO5	3	3	3	2	3	3	3

Paper Code: ADVANCED EMBEDDED SYSTEMS LAB
Paper Code: MEC291
Contact hours: 36
Credits: 2

COURSE OUTCOMES:

After the completion of this lab, Students should be able:

- To create the hierarchical decomposition of sequential designs.
- To perform synthesis and analysis of embedded system.

Sl.NO	Experiments
	Write a C Program for the following
1	To Test 4X4 keypad using Cortex M3 microcontrollers.
2	To Display message on Graphic LCD display using Cortex M3 microcontrollers.
3	To Test working on Internal ADC using Cortex M3 microcontrollers.

4 To Test working of Internal DAC using Cortex M3 microcontrollers.

5 To test working of Interrupt using Cortex M3 microcontrollers.

6 To test on PWM technique using Cortex M3/M4 microcontrollers.

Write an assembly language program using suitable CAD software/Tools

7 To link multiple object files and link them together

8 To locking a Mutex

9 Write a SVC handler in C. Use the wrapper code to extract the correct stack frame starting location. The C handler can then use this to extract the stacked PC location and the stacked register values.

10 Write a C-program for FCFS First come first serve using suitable CAD software to present the Output of CPU Scheduling algorithm.

11 Write a C-program for SJF Shortest job first using suitable CAD software to present the Output of CPU Scheduling algorithm

12 Write a C-program for Priority using suitable CAD software to present the Output of CPU Scheduling algorithm

TOTAL:36 PERIODS

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	3	2	2	1	3	2
CO2	3	3	3	3	1	3	3

Paper Code: VLSI SIGNAL PROCESSING LABORATORY
Paper Code: MEC292
Contact hours: 36
Credits: 2

COURSE OUTCOMES:

CO1 Perform basic signal operations and verify fundamental DSP concepts such as signal generation, sampling, and transformations.

CO2 Implement linear and circular convolution, auto-correlation, and cross-correlation techniques in time and frequency domains.

CO3 Analyze and compute DFT, IDFT, and FFT of signals and apply them to practical DSP scenarios.

CO4 Design and implement digital filters in real-time using DSP processors such as TMS320C67xx or ARM Cortex series.

CO5 Apply DSP algorithms to basic image processing tasks and evaluate system-level performance using advanced signal processing platforms.

EXPERIMENTS:

1. Basic Signal Operations- Generation and Plotting of Signals (Sine, Cosine, Square, Triangular, Exponential, etc.) Operations on Signals Sampling Theorem Verification (NyquistCriterion)
2. Linear Convolution and Circular Convolution

3. Auto-correlation and Cross-correlation
4. Computation of DFT & IDFT
5. FFT Algorithm Implementation
6. Implementation of Filters in Real-Time using DSP Processors
7. Z-Transform and Inverse Z-Transform
8. Implementation of DSP Algorithms using TMS320C67xx or ARM Cortex DSP Processors
9. Image Processing

TOTAL:36 PERIODS

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	3	2	2	2	–	2	2
CO2	3	3	2	2	–	3	2
CO3	3	3	3	2	–	3	2
CO4	3	3	3	3	1	3	3
CO5	3	3	3	3	1	3	3

SEMESTER III

Paper Code: ASIC DESIGN
Paper Code: MEC301
Contact hours: 36
Credits: 3

COURSE OUTCOMES:

Upon completion of this course, the students will:

1. Be able to design the ASIC implementation using programmable ASIC devices.
2. Be able to comprehend the different issues related to the development of ASIC designs including logic synthesis, floor-planning, placement and routing, tools and future trends.
3. To study the basic concepts of digital CMOS Application Specific Integrated Circuit (ASIC) systems design and library cell design.
4. To know the architectural details of programmable ASICs.
5. To present the ASIC physical design flow, including logic synthesis, floor-planning, placement and routing.
6. To know back-end physical design flow steps through VLSI CAD tools.

MODULE I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 7L

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell — Sequential logic cell - Data path logic cell - Transistors as Resistors — Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

MODULE II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS **7L**

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA – Altera FLEX- Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

MODULE III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY **8L**

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 — Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

MODULE IV LOGIC SYNTHESIS, SIMULATION AND TESTING **8L**

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

MODULE V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING **6L**

System partitioning - partitioning methods - floor planning - placement - physical design flow — Routing - global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL:36 PERIODS

REFERENCES:

1. M.J.S .Smith, "Application Specific Integrated Circuits", Addison - Wesley Longman Inc., 1997, Reprint 2004.
2. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.
3. Wayne Wolf, "FPGA-Based System Design", Prentice Hall PTR, 2004.
4. R. Rajsuman, "System-on-a-Chip Design and Test. Santa Clara, CA: Artech", House Publishers, 2000
5. F. Nekoogar. "Timing Verification of Application-Specific Integrated Circuits (ASICs)", Prentice Hall PTR, 1999.

	PO1	PO2	PO3	PO4	PO5	PSO1	PSO2
CO1	2	3	3	2	1	3	2
CO2	2	3	3	2	1	3	2
CO3	3	2	2	2	1	3	2
CO4	2	2	2	1	1	2	2
CO5	2	3	3	3	1	3	2
CO6	2	2	3	3	1	3	2

- **PROGRAM ELECTIVE (SWAYAM/NPTEL BASED)**

Students may earn credits through SWAYAM/NPTEL courses as approved and mapped by the Board of Studies.

OPEN ELECTIVE (SWAYAM/NPTEL BASED)

Students may earn credits through SWAYAM/NPTEL courses as approved and mapped by the Board of Studies.

A) Business Intelligence & Analytics (SWAYAM/NPTEL)

Course Objectives

- **To understand fundamentals of data analytics and business intelligence.**
- **To apply analytical tools for data-driven decision making.**

Course Content (Indicative Topics)

Introduction to Business Intelligence; Data Warehousing concepts; Data Mining techniques; Predictive analytics; Statistical tools; Data visualization; Decision support systems; Case studies.

Course Outcomes

CO1: Apply data analytics techniques for business decision making.
CO2: Analyze large datasets using BI tools.
CO3: Interpret results for strategic planning.

B) Industrial Safety Engineering (SWAYAM/NPTEL)

Course Objectives

- **To understand principles of industrial safety and risk management.**
- **To analyze hazards and implement safety measures in industrial systems.**

Course Content (Indicative Topics)

Industrial safety regulations; Hazard identification and risk assessment; Safety management systems; Accident analysis; Fire safety; Electrical safety; Occupational health and safety standards; Safety audits.

Course Outcomes

CO1: Identify industrial hazards and associated risks.
CO2: Apply safety standards and regulations in engineering practice.
CO3: Develop safety management strategies.

Course Name: DISSERTATION / RESEARCH PROJECT / INTERNSHIP (PART–I)
Course Code: MEC381
Credit: 10

Course Objectives

- **To identify a research problem in the relevant specialization area.**
- **To conduct literature survey and define research methodology.**
- **To initiate preliminary design/implementation/analysis work.**

Course Content

Problem identification; Literature survey; Formulation of objectives and methodology; System modeling/design; Experimental setup/Simulation studies; Preliminary results; Periodic review and presentation.

Course Outcomes

CO1: Identify and formulate a research problem.
CO2: Conduct literature review and prepare technical documentation.
CO3: Demonstrate initial research findings through presentation and report submission.

Course Name: DISSERTATION / RESEARCH PROJECT / INTERNSHIP (COMPLETION - PART–II)

Course Code: MEC481
Credit: 10

Continuation and completion of the research work initiated in Part–I, including detailed design/implementation, experimentation/simulation, data collection, performance analysis, validation of results, and optimization. Preparation of dissertation report in prescribed format. Submission of research paper to peer-reviewed journal/conference (desirable). Final presentation, viva-voce examination, and demonstration of the developed system/prototype

Course Outcomes
CO1: Design and implement a solution to a complex engineering/research problem.
CO2: Analyze experimental/simulation results and draw valid technical conclusions.
CO3: Demonstrate the ability to conduct independent research with ethical standards.
CO4: Prepare and present a comprehensive technical dissertation.
CO5: Publish/present research findings in professional forums (desirable outcome).